In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Canceled)

2. (Previously Presented) A method as defined in claim 3, wherein the spacers are formed by depositing and etching a SiN layer.

3. (Currently Amended) A method of fabricating a memory cell comprising:

forming spacers to isolate and protect a gate area including a floating gate and a control gate;

forming a gap filling layer over a substrate including the gate area and the spacers, wherein the gap filling layer is formed by depositing undoped polysilicon or amorphous silicon, wherein the gap filling layer fills a narrow gap between adjacent gate areas without any voids;

performing an anisotropic etching of the gap filling layer, wherein the gap filling layer remains in the narrow gap without being substantially removed by the anisotropic etching; and

depositing an insulating layer over the gate area and the gap filling layer~~, wherein the gap filling layer is formed by depositing undoped polysilicon or amorphous silicon~~ over the gate area and the spacers~~, and by performing an anisotropic etching of the deposited undoped polysilicon or amorphous silicon~~.

4. (Previously Presented) A method as defined in claim 3, wherein the insulating layer is formed of TEOS (tetra ethyl ortho silicate) or BPSG (borophosphorsilicate glass).

5. (Canceled)

6. (Previously Presented) A memory cell structure as defined in claim 7, wherein the spacers are formed of SiN.

7. (Currently Amended) A memory cell structure comprising:

a substrate including N-well, P-well, and source/drain region;

a plurality of gate areas formed on the substrate, the gate areas including a gate oxide, a floating gate, an insulating layer, and a control gate;

spacers on sidewalls of the gate areas;

a gap filling layer formed without any voids in narrow gaps between the spacers of the gate areas adjacent gate areas; and

an insulating layer deposited over the gate areas, and the gap filling layer, and an exposed surface of the substrate, wherein the gap filling layer is formed of undoped polysilicon or amorphous silicon.

8. (Original) A memory cell structure as defined in claim 7, wherein the gap filling layer is formed by an anisotropic etching.

9. (Canceled)

10. (Canceled)

11. (New) A method as defined in claim 3, wherein performing an anisotropic etching of the gap filling layer etches a predetermined part of the gap filling layer to expose a surface of the substrate.

12. (New) A memory cell structure as defined in claim 7, wherein the narrow gaps between adjacent gate areas are located above the source/drain region in the substrate.